Project for Energy Storage on a Chip for MEMS

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Abstract

A new project with a budget of 262 thousands Euro was motivated by the lack of micromachined energy storage solutions that can be integrated with a MEMS harvester on a chip with a specific circuitry. . These key components of the system are highly needed for autonomous microsystems and have to be integrated to enable an energy-autonomous, but efficient operation The targeted energy storage device needs to be charged very slowly from harvesters with output energies in the µWs range. As a consequence, tailored materials and technologies for the realization of thin-film capacitors compatible with CMOS technology are of utmost importance. Target capacitance value about one hundred µF/cm^2, low loss factor and low leakage currents are the expected properties of these devices.

Introduction

Energy storage for MEMS harvesters integrated on a chip with a specific circuitry is a key feature for the successful operation of autonomous micro systems. Integration of the energy storage on a chip conditions the when targeting CMOS compatibility. The idea of energy storage on a chip is based on utilizing the back side of the silicon die. By exploiting the full chip area will help to create capacitors of enough high capacitance values. One electrode of the capacitor will be connected to the chip electronics, the second one with ground via e.g. package as it is shown in Fig. 1. The proposed capacitor is suitable for integrated MEMS harvesters based on e.g. piezoelectric, thermoelectric and electrostatic approach. Due to their low output currents, ultra-low loss factors as well as leakage current levels need to be assured. Current technologies offer low capacitance (MOS capacitor) or high leakage currents or an encapsulated electrolyte e.g. for electrochemical supercapacitors, thus making the latter approach technologically most challenging. A rough estimation of the generated energy from low power harvesters is about 100 nW. When the supply voltage will be 5 V, then the charge will be about 72 µC/hour. A capacitance of 15 µF will be necessary to store this amount of charge. Due to the direct consumption, efficiency of conversion below 5 V and self-discharging, a capacitance between 100-200 µF is needed to store the generated energy on a daily basis.

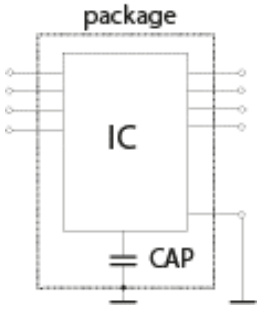

Fig. 1: Schematic block diagram of an integrated circuit and an energy capacitor in one package.

Technology state of the art

The standard MOS capacitor was developed for integrated circuits. It is made of a semiconductor formed by a heavily doped n+ poly-silicon layer as one electrode. Silicon oxide (SiO_2) as a gate dielectric has seen tremendous improvements in CMOS technology over the last few decades yielding high quality insulation with ever decreasing film thickness. At the beginning of the MOS technology the thickness of dielectric was about 1000 Å and capacitance tens of nF/cm^2 enabling to create capacitors on a chip of about tens pF. Current technologies use less than 20 nm of dielectric thickness and capacitors of hundreds of pF. The MOS capacitor is a MIS structure which makes its capacitance depending also on the applied voltage. The fundamental thickness limitation of SiO_2 is given by increasing tunnelling leakage currents, prompting a search for alternative dielectric materials with higher dielectric constants ε_r compared to SiO_2 (so called high-k dielectrics) [1- 3]. Since the dielectric response at typical frequencies used in CMOS devices is mainly dominated by ionic and electronic polarization, potential candidates can be found in material systems where heavy metals with a large number of electrons (e.g. transition metals like Ta, Nb, Hf, Zr) form ionic bonds to oxygen. Figure 2 shows common high-k dielectrics. It is apparent, that there is a compromising relationship between the static dielectric constant, the bandgap E_g and the electrical breakdown field strength E_{bd}.

Given these requirements, promising dielectrics for on chip energy storage are Ta_2O_5, HfO_2 and ZrO_2, combining high dielectric constants and low leakage currents. Ta_2O_5 (as well as $SrTiO_3$) undergoes deleterious reactions with an underlying silicon substrate at high temperatures of ~700°C [4, 5], thus a low temperature oxidation step for porous tantalum thin films will be necessary. Amorphous tantalum pentoxide prepared by anodization presents good dielectric properties (dielectric constant of 25–27) complemented by high thermal, chemical and long term stability [6, 7]. ZrO_2 is isomorphous to HfO_2, but it is slightly unstable and can form $ZrSi_2$ with silicon [8]. HfO_2 exhibits a high thermal stability and is therefore a very promising candidate for this application, but it exhibits a significantly lower dielectric constant compared to Ta_2O_5.

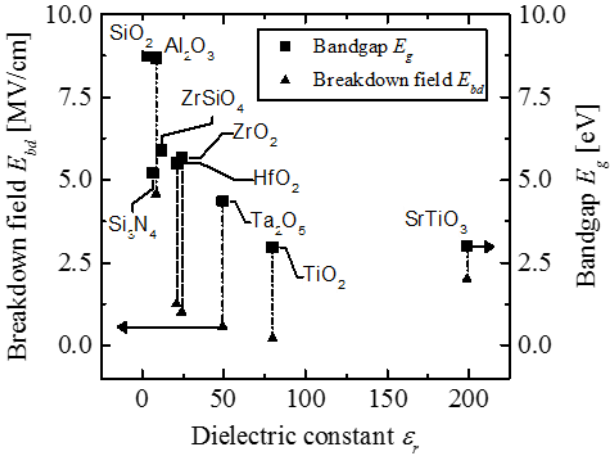

Fig. 2: Dielectric constant, bandgap and breakdown field strength of selected dielectrics [1].

IPDiA has developed 3D silicon capacitor based on SiO_2 dielectric using deep structures. The technology capability is determined by density of 250 nF/mm^2 and properties such as reliability and stability up to 200°C, low temperature coefficient, low ESR, low ESL, and leakage current down to 100 pA. Deep Reactive Ion Etching (DRIE) is standard technique using so called Bosch process to obtain deep structures (pores or columns) followed by Atomic layer deposition of dielectric film. Lower electrode is highly doped silicon film, top electrode is purely metallic or as bilayer with poly-crystalline silicon stack. 2D and 3D structures prepared by photo-electrochemical etching were also demonstrated. This wet technique uses electrochemical etching in hydrofluoric acid (HF), where pores grow in perpendicular to the surface direction and pore walls become passivated against dissolution. The process is supported by photo-generation of minority carries from the backside of the wafer using UV lamp [9]. Another technique uses randomly formed mask for Si etching to obtain high aspect ratio structure [10]. Porous structure has not uniform shape after HF etching (Fig. 3).

Other techniques do not use silicon etching. A very promising technique for the realization of deep porous structure is unconventional approach using sputtering of Ta film forming spontaneously directly to columns. Advantage of the structure is a simple oxidation procedure of Ta to form a dielectric film on the structure [11]. Mozalev

demonstrated two different approaches: i) formation of porous alumina covered with an anodic film of Ta and ii) anodization of bilayer Al/Ta to grow nanopillars of Ta_2O_5. The first approach was published in [12] as an on-chip

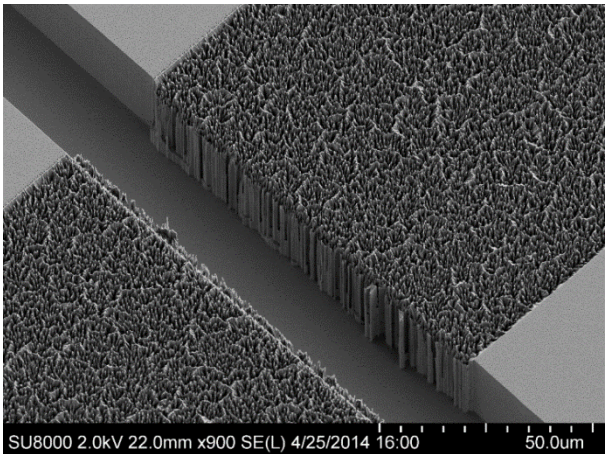

Fig. 3: Porous electrode structures of an electrolyte based supercapacitor in the device layer on a SOI wafer.

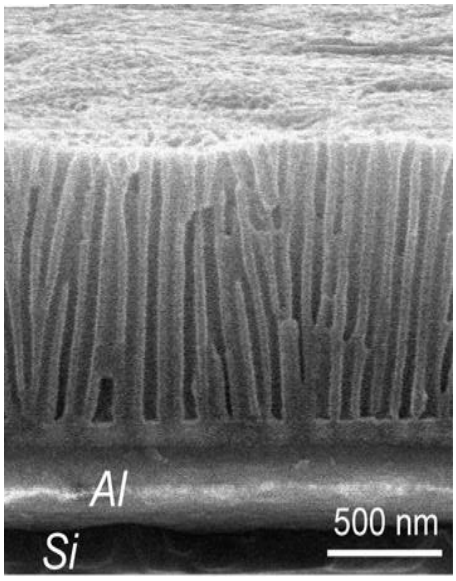

Fig. 4: SEM cross-sectional micro-graph of Al/Ta sputtered film anodized at 51 V [10].

high-frequency integral capacitor. The aluminium was consumed by anodization to generate a ~1 μm thin porous mask. Tantalum oxide was formed on sputtered Ta film in the porous alumina (Fig. 4). The leakage currents resulted in the range of $(3–20)\cdot10^{-12}$ A mm^{-2}. Obtained capacitance values of 6.4 nF cm^{-2} are still low for energy storage applications, but other parameters such as low leakage current levels are very promising.

The project aim

Ultra-low-power systems or even zero-power systems are developed for implantable, mobile and wearable applications. Typically, these applications require the full integration of energy autonomous systems which besides the electronics also comprise components as key elements generating energy for their power supply. Therefore, integrated circuits and energy harvesters are integrated together with the help of microtechnologies. Another key component still missing to date is energy storage offering the capability to be integrated on a chip. Such solution is of utmost importance for an energy autonomous operation of the system because micromachined harvesters generate low immediate power which has to be stored for later use or the energy is generated for partial time only and has to be accumulated for operational periods where e.g. data are collected by sensors, conditioned by electronics on a chip level and sent wirelessly to a data base for final evaluation. Integration of miniaturized capacitors with a capacity of uF to mF within the mentioned systems is highly desired. This project aims to close this gap by developing adequate CMOS or MEMS compatible technologies and methodologies for on-chip integration of capacitors based on high-k dielectrics. We expect to created such devices using developed technologies with target capacitance value of about 100 μF/cm^2, loss factor in the level of 10^{-3} and leakage currents below 10^{-11} A/mm^2.

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