3.3. A New Approach to the Design of High Precision Integrated Resistive Voltage Dividers

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ABSTRACT

The simplest realisation of an integrated voltage divider is two resistor elements in series on a single substrate with a termination connecting to each of the three nodes. For high precision requirements metal foil or metal film technology offers intrinsically high precision properties, and for low voltage ratios the ratio tolerance can typically be down to 0.05% and tracking TCR to 2ppm/K. However, when a requirement for high voltage is added to the mix, this challenges the precision for two reasons. Firstly, it forces the adoption of thick film technology at least for the high voltage element, and this has poorer tolerance and TCR. And secondly, the ratio between resistor values is generally much greater, making matching of TCR and drift characteristics more difficult.

The methods currently used to mitigate these challenges to precision are generally focused on two areas. The first is to improve the absolute tolerance and TCR of thick film materials by material or process development. The second is to use component matching to yield higher precision and TCR tracking, either by switching to discrete matched parts, or by assembling an integrated component by attaching together two substrates.

This paper describes a third method of reconciling high voltage with high precision which is based on a re-design of the voltage divider at the schematic level. It shows how, by dispensing with the conventional two-element approach, an alternative design methodology promises to achieve high levels of precision with conventional thick film materials and processes and without the high cost of component matching.

EXISTING METHODS OF RESISTIVE VOLTAGE DIVISION

Principles of the Conventional Design

A conventional high voltage divider consists of two resistive elements: a high voltage leg R_1 and low voltage leg R_2. Figure 1 shows a typical application in which the output of a high voltage source is scaled down and fed back for measurement or regulation purposes. Assuming that the input impedance of the buffer is much greater than R_2 the loading on the divider is negligible, so the voltage ratio is simply given by:

1. $$\frac{V_i}{V_o} = \frac{R_1+R_2}{R_2} = \frac{R_1}{R_2} + 1$$

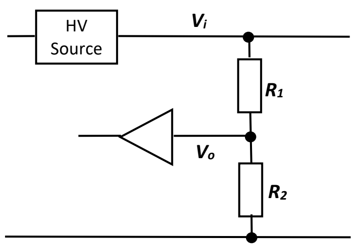

Figure 1 – Conventional Voltage Divider

The accuracy of voltage division ratio therefore depends on the ratio between resistor values rather than on the absolute values. In thick film technology the practical limit lies around 0.1% tolerance and 25ppm/K temperature coefficient of resistance (TCR). The optimum accuracy of voltage division ratio may be obtained in a monolithic divider for which the manufacturer can guarantee the extent to which the vales are in the desired ratio (ratio tolerance) and the extent to which the TCRs match (tracking TCR.)

Example Applications

High voltage divider applications are found wherever a voltage must be monitored or regulated which is at a high level inconsistent with analogue control circuitry, or the ADC stage of a digital system. Three examples from different end markets are as follows.

1. Energy metering – smart electricity meters contain a voltage measurement function which feeds into the energy usage calculation. This is normally achieved with a series string of typically 6 to 10 metal film MELF parts for the high voltage resistor. The typical divider requirements here are 264V input, 50:1 ratio, input impedance of 1 megohm, tracking TCR of 25ppm/K and ratio stability of 0.1%. Linearity related to VCR is not so critical as only a narrow range of voltages needs to be measured, but there is also the need to withstand lightning strike induced surges up to 10kV, and thick film is a better technology than metal film for this purpose.

2. Automotive – in an EV with an 800V battery a "gas gauge" function requires voltage measurement which calls for a divider with a 1kV input rating, 200:1 ratio and around 5 megohms input impedance. Tracking TCR of 10ppm/K, tracking VCR of 1ppm/V and 0.1% stability are needed. The harsh environmental conditions, and especially the potential for high humidity, make thick film technology the ideal choice, if it can be pushed to meet the precision requirements.

3. Medical – an automatic external defibrillator (AED) controls the energy dose delivered to the patient by adjusting the charging voltage of the main capacitor. The measurement of this voltage is therefore a critical function and is performed by a divider with at least a 5kV rating and, to keep self-heating low, the input impedance may be around 50 megohms. The precision requirements are typically tracking TCR of 25ppm/K, tracking VCR of 2ppm/V and 0.1% stability. For tropical installations the humidity performance is once again critical and thick film is normally used.

It is worth pointing out that the ratio tolerance has been left out of these specifications. Often, for conventional dividers, this can easily be specified at 0.1%, but this is not essential for such applications as all use software-based calibration of the voltage ratio during manufacture. In principle therefore, a ratio tolerance of 5% or even more could be accommodated.

Limitations of the Conventional Design

The ohmic value of a film resistor is the product of its resistivity in Ω/square and the track length measured in squares. Therefore, R_1 is commonly formed by a long, thin meander of many squares in length, whilst R_2 is a small block pattern element of close to one square. To achieve a high ratio of resistances in the range of hundreds up to tens of thousands cannot be done by geometry alone; it requires different materials with different resistivities for R_1 and R_2. Inevitably these have different values of TCR and voltage coefficient of resistance (VCR). Furthermore, they are generally formed with different geometries also, and so exhibit parasitic reactive impedances, the magnitudes of which do not necessarily match the resistance ratio, and different end effects in the region adjoining the conductor material. These factors make the voltage ratio sensitive to changes in temperature, applied voltage and applied frequency. Furthermore, under long-term electrical and environmental stress conditions, the permanent value changes in the two resistor elements will generally be dissimilar, leading to permanent drift in voltage ratio during operational life.

Mitigated Designs

In an attempt to push thick film high voltage dividers to the limit of accuracy manufacturers have used proprietary thick-film materials with enhanced levels of homogeneity and very tight process control to reduce or control TCR characteristics. Also, the screen-printing normally used to create the thick film patterns may be replaced by an additive direct application or "writing" process to achieve higher square counts, permitting the use of lower resistivity films with lower TCR and VCR figures [1].

In some products the process resorts to a grading and sorting strategy where R_1 and R_2 are formed on separate substrates then graded by value and TCR. Pairs of matching elements are then joined with adhesive to make a quasi-monolithic component with optimum ratio tolerance and tracking TCR.

All of these strategies bear significant yield and cost disadvantages, which means that the highest accuracy dividers are employed only in niche applications where the added value is deemed affordable.

Definition of Terms

To continue discussion of voltage dividers and prepare for the alternative design method to be described, two new terms need to be proposed. These are:

1. Temperature Coefficient of Voltage Ratio (TCVR) is the reversible change in the voltage ratio due to changes in temperature and is expressed in ppm/K. In a conventional divider design, the tracking TCR is used to characterise this parameter.

2. Voltage Coefficient of Voltage Ratio (VCVR) is the reversible change in the voltage ratio due to changes in input voltage and is expressed in ppm/V. In a conventional divider design, the tracking VCR is used to characterise this parameter. Note that, unlike VCR of a single resistor which is always negative, VCVR may be positive or negative.

State of Art Benchmark

A datasheet analysis was performed of the major suppliers of thick film high voltage dividers, with particular regard to the three key aspects of precision, TCVR, VCVR and life drift. The results are indicated in Table 1, which also includes the design to be described, identified here as CBD, for comparison. With regard to TCVR and VCVR, this reflects actual results, and with regard to life drift it reflects the design goal, life drift testing not having been performed at time of writing.

Supplier	TCVR (±ppm/K)	VCVR (±ppm/V)	Life Drift (%)	Notes
A	2	0.02	0.02	Match & Join Process
A	5	0.02	0.02	Match & Join Process
A	5	0.02	0.04	Match & Join Process
B	5	0.05	0.15	Match & Join Process
C	10	0.2	0.5	Conventional
D	10	0.05	0.2	Writing Process
E	10	1	2	Conventional
F	10	2	4	Conventional
A	10	1	0.4	Conventional
G	15	15	0.5	Conventional
H	25	0.15	0.5	Conventional
C	25	0.4	0.4	Conventional
I	25	1	0.3	Conventional
I	25	1	0.3	Conventional
J	25	1	0.5	Conventional
K	50	5	4	Conventional
CBD	5	0.2	0.1	CBD Design

Table 1 – Comparison of Current Market Offerings by Precision Parameters

This comparison may be better understood by reference to Figure 2 which indicates the locations on a TCVR / VCVR plane with life drift indicated by bubble area. This also indicates the design and processing used by the different products categories.

Dividers with conventional design and process are the most common and offer precision up to 10ppm/K, 0.2ppm/V and life drift of 0.3%, although 25ppm/K, 1ppm/V and 0.5% are more typical values. Direct writing process for thick film application delivers a fourfold improvement in VCVR whilst the matching strategy offers nearly a decade improvement in both TCVR and VCVR.

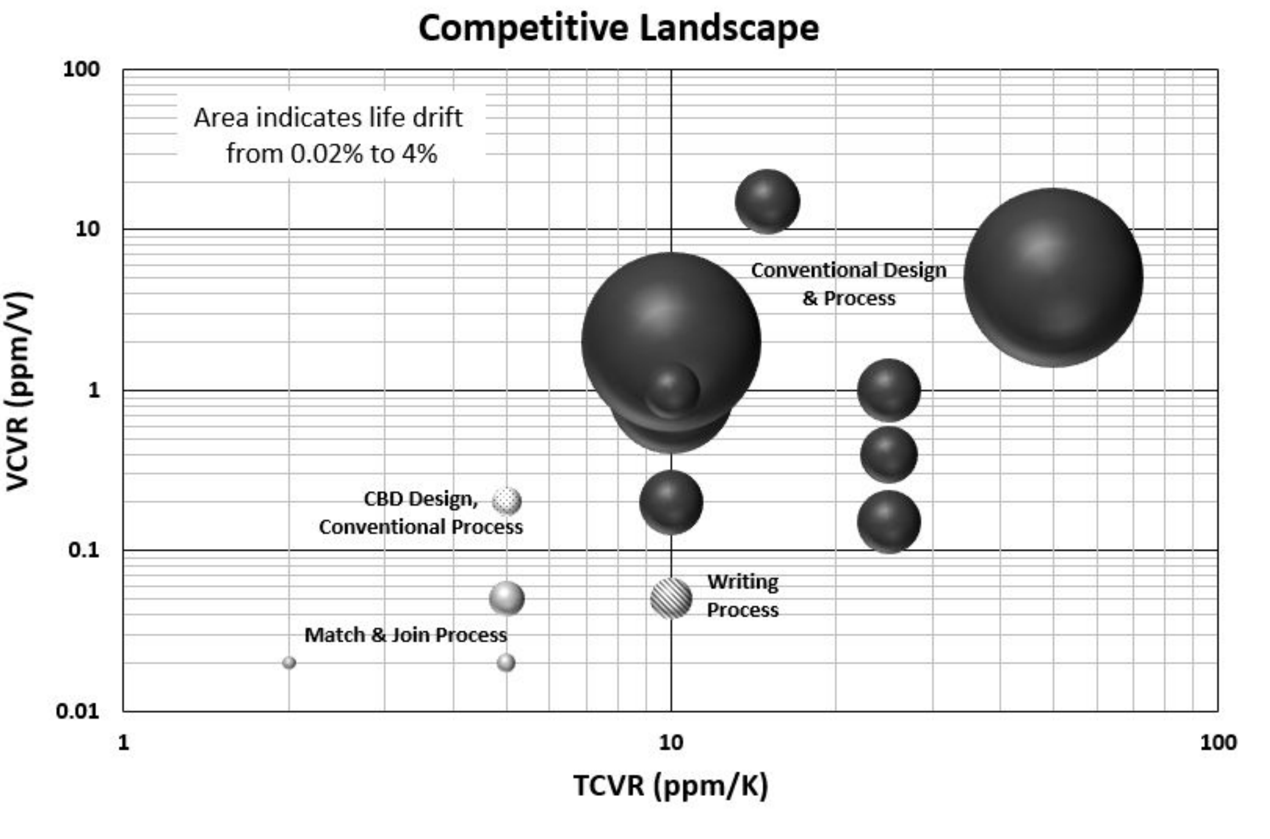

Figure 2 – Comparison of Current Market Offerings by Precision Parameters

Further analysis of divider properties investigated the relationship between product ratings and precision. It is well known that the resistivity drift seen in thick film materials is strongly influenced by operating temperature. A strategy for improving stability therefore is to de-rate the product so that self-heating and voltage stress are both reduced.

The correlation between drift and power density is very clear when these parameters are plotted as shown in Figure 3. The power density was simply calculated from the datasheet power rating divided by the total substrate area, and the drift was taken from the datasheet environmental test performance limits.

This reveals the extent to which the very low drift figures offered by the match and join process products is the result of rating the products at very low power and voltage relative to the product dimensions. It is likely to be the case that to approach the same drift levels in the design to be described, control of power density will be a factor that needs to be considered, and restriction of ratings will be required.

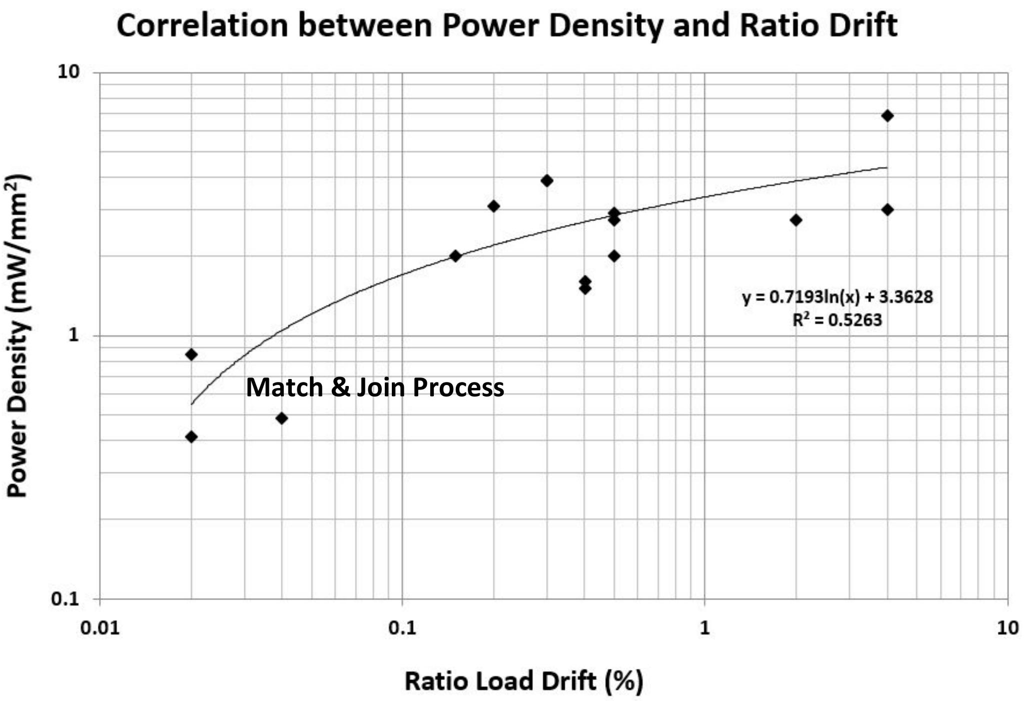

Figure 3 – Ratio Drift Reduction through Limiting Power Density

A NEW APPROACH

The Kelvin Varley Circuit

An alternative resistive voltage division circuit exists within the realms of laboratory standards in the form of the Kelvin Varley circuit [2], [3]. This is based on the concept of using multiple identical sub-elements for each resistor thereby enabling a very high level of linearity and ratio stability to be achieved. An iterative approach is used whereby divider stages formed in this way are cascaded to provide multiple levels of division allowing several digits of resolution for the division ratio. The circuit is generally made switchable so that any desired division ratio may be set within the resolution of the instrument.

Figure 4 shows the principle of operation. In this example the division ratio is set to 0.3184 i.e. 3.141:1, and correct circuit operation relies on zero output loading, either by high impedance buffering or by a nulling strategy. This circuit is the standard solution for low voltages and relatively low voltage ratio division at a selectable ratio.

Some but not all aspects of this circuit are useful for the task of creating a high precision high voltage divider. The use of multiple identical sub-elements provides the balance necessary to achieve good linearity. This strategy alone however would require a number of sub-elements equal to the required voltage ratio, which would be impractical for ratios in the 100 to 10000 range. The second aspect is the cascading of multiple stages which allows high ratios to be achieved with a manageable number of sub-elements. The aspects that are not applicable are the switchability and the use of high interstage loading. Nevertheless, this division technique forms the background to the new design approach described here.

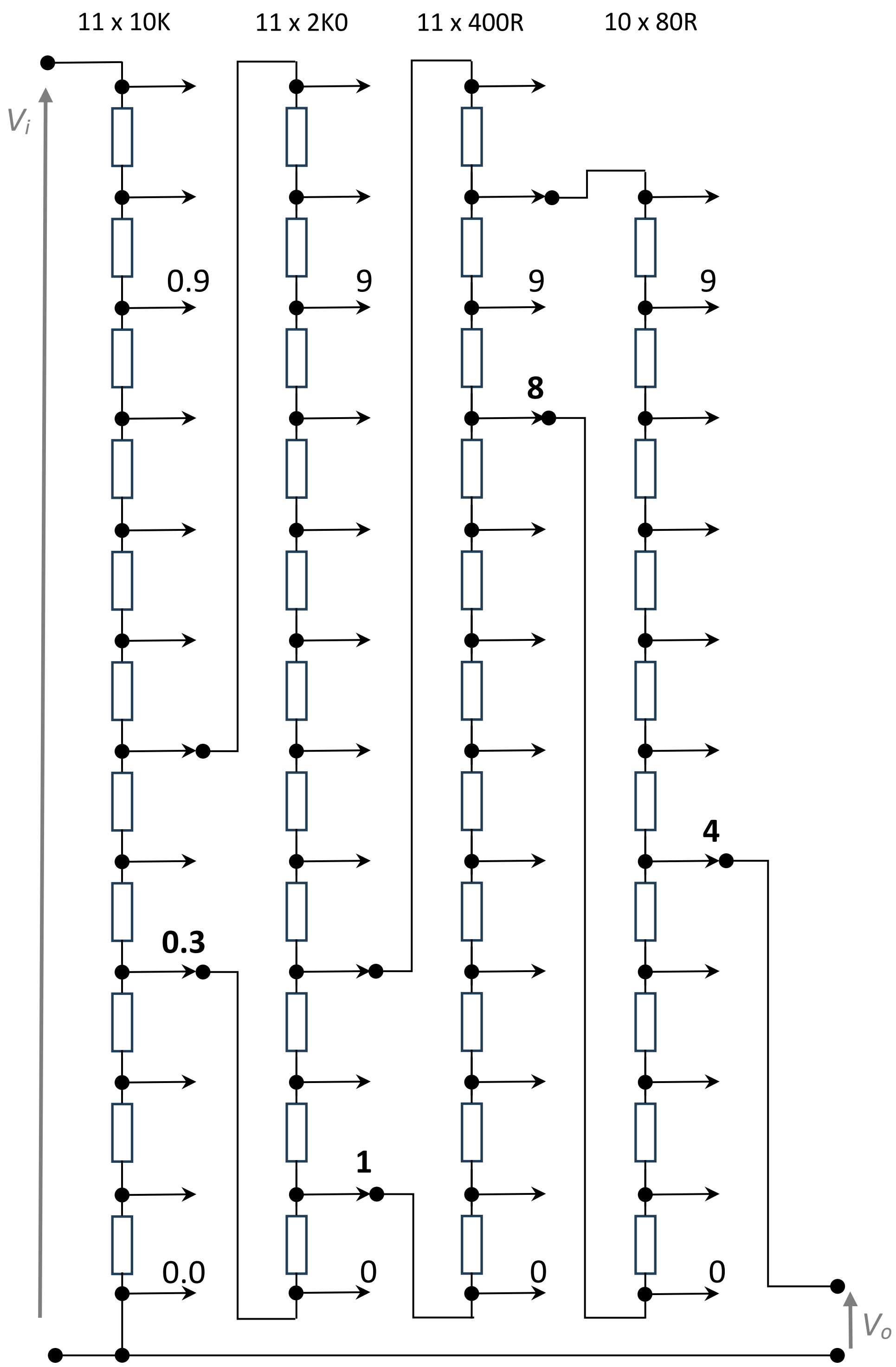

Figure 4 – Schematic the Kelvin Varley Divider Set to a Ratio of 1:0.3184

Monolithic Cascaded Balanced Divider (CBD)

This new approach aims to provide a high voltage division ratio by providing two or more cascaded voltage divider stages, each having moderate ratio, such that the overall divider ratio is approximately equal to the product of the individual ratios. Each stage is designed with a series of N identical elements, each with the same terminations, geometry and material (Figure 5). Each cascaded stage consists of multiple balanced elements, so the term Cascaded Balanced Divider (CBD) was chosen.

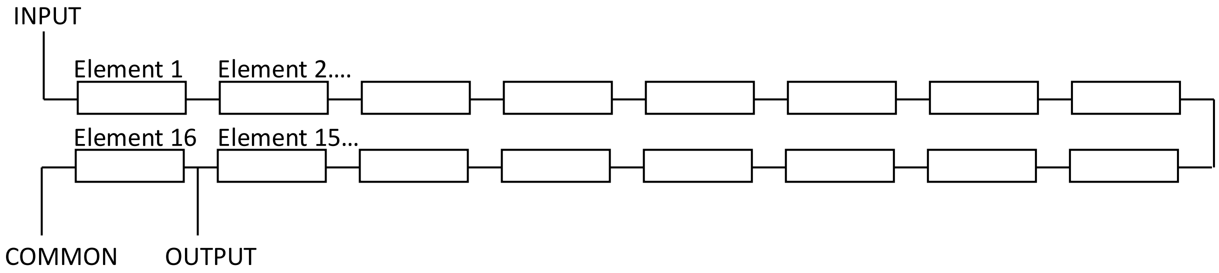

Figure 5 – Schematic of 16-Element Voltage Divider Stage

The elements 1 through (N-1) form the high voltage leg R_1 and element N forms the low voltage leg R_2. This represents a resistance ratio of (N-1):1 and corresponding voltage division ratio of N:1. The output of this divider is connected to a second divider (R_3 and R_4), which is designed using the same principles as the first (see Figure 6). The resistance values selected may optionally be the same ($R_3 = R_1$ and $R_4 = R_2$), but in any case, must have $(R_3 + R_4) >> R_2$ to prevent excessive loading of the second divider by the first. In general, the second divider may be made physically smaller than the first as it has less voltage stress and, if significant, lower power dissipation. Note that different geometry and higher resistivity materials may be used in the second divider compared to those used in the first in order to facilitate this. What matters is the matching of elements within each divider. It will later be shown that matching elements between dividers is much less important.

As an example, the number of elements per divider stage may be 33, which gives a voltage division ratio for two stages of around 1000:1. The number of stages may be extended to give higher total voltage ratios, and / or to permit lower stage ratios. However, best performance is achieved with a minimum number of stages, each with the maximum practical stage ratio.

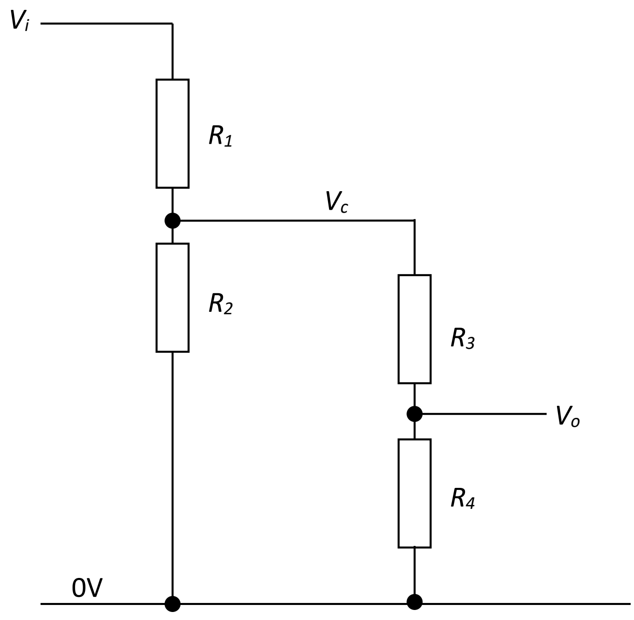

Figure 6 – Two-Stage Cascaded Balanced Divider

For the two-stage cascaded divider of Figure 6, the voltage ratio of the first stage, if disconnected from the second, is given by:

2. $$V_c = \frac{V_i.R_2}{R_1+R_2} = \frac{V_i}{1+R_1/R_2}$$

Similarly, the voltage ratio of the second stage, assuming no significant output loading, is given by:

3. $$V_o = \frac{V_c}{1+ R_3/R_4}$$

The combined voltage ratio, allowing for the loading of the first stage by the second stage, is given by:

4. $$V_o = \frac{V_i}{(1+R_1/(R_2||(R_3+R_4)).(1+R_3/R_4)}$$

where || indicates the parallel combination of ohmic values, i.e. $R_2||(R_3 + R_4) = (R_2^{-1} + (R_3 + R_4)^{-1})^{-1}$.

If the value $(R_3 + R_4) >> R_2$ this may be simplified to:

5. $$V_o = \frac{V_i}{(1+R_1/R_2).(1+R_3/R_4)}$$

This is to say, the combined voltage ratio approximately equals the product of the individual stage ratios.

In practice the ability to select values such that $(R_3 + R_4) >> R_2$ is constrained by two considerations. Firstly, values of R_1 and R_2 which are too low would result in excessive power dissipation. Secondly, very high values of R_3 and R_4 may be undesirable because they would entail the use of extremely high resistivity materials, which are associated with poorer absolute TCR and stability. However, there is scope within the wide value range of thick film technology to balance these constraints with the need to minimise inter-stage loading.

So, ignoring for now the inter-stage loading, for the ideal case represented by equation 5, the voltage ratio V_o:V_i is sensitive only to changes in the individual stage resistance ratios R_1:R_2 and R_3:R_4, and this has been minimised by the balanced stage design. There is no sensitivity to the ratio $(R_1 + R_2)$:$(R_3 + R_4)$, so the two divider stages may be allowed to differ in TCR, VCR, parasitic reactive impedance and ageing drift, without affecting the voltage ratio.

Furthermore, it may be assumed that the individual stage resistance ratio errors $\Delta(R_1$:$R_2)$ and $\Delta(R_3$:$R_4)$ are statistically independent, so that the corresponding error in voltage ratio is given by the root of the sum of the squares:

6. $$\Delta(V_o\colon V_i) = \sqrt{(\Delta(R_1\colon R_2)^2 + \Delta(R_3\colon R_4)^2)}$$

For example, a 1ppm error in both resistance ratios will result in a $\sqrt{1^2 + 1^2} = 1.41$ppm error in voltage ratio.

Now considering inter-stage loading by extending this to the general case of equation 4, there is additional sensitivity to the ratio $(R_1 + R_2)$:$(R_3 + R_4)$, and this has not been minimised by design. However, the effect is approximately divided by the factor R_2 / R_3. For example, a 100ppm change in the ratio $(R_1 + R_2)$:$(R_3 + R_4)$ where $R_3 = 100.R_2$ will result in a 1ppm change in the voltage ratio V_o:V_i. This may be combined with the above calculated errors to give for this example case $\Delta(V_o$:$V_i) = \sqrt{1^2 + 1^2 + 1^2} = 1.73$ppm.

This analysis may be extended to three stages, allowing voltage ratios over 30,000:1 to be achieved, meeting the majority of practical applications.

Interstage Sensitivity Analysis

A 3-stage divider with a 200:1 ratio was made in PartSim to test the sensitivity of the voltage ratio to mismatches in TCR or value drift between stages. In general, the design method does not attempt inter-stage matching but mitigates its effects by minimising the loading on each stage by the one that follows. Figure 7 shows the initial design in the first schematic. The second schematic shows the effect of increasing the ohmic values in stage 2 only.

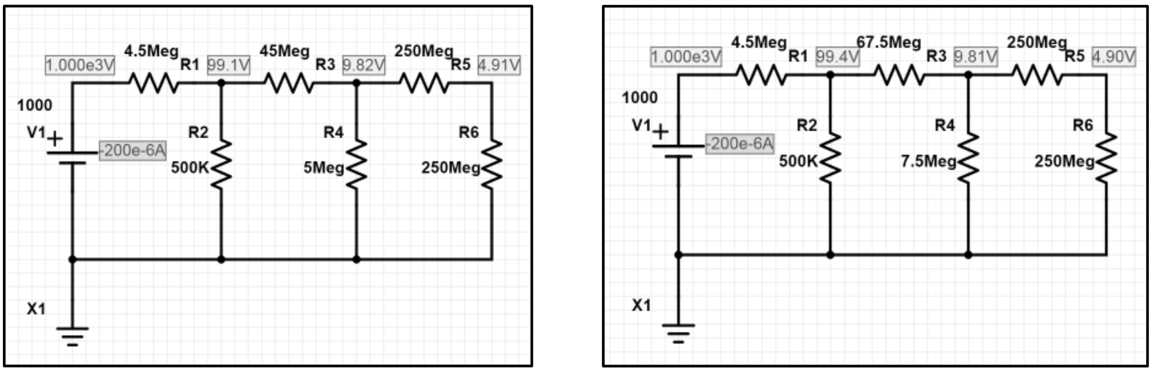

Figure 7 – PartSim Simulations to Test Inter-Stage Sensitivity

The result was that changing the values in stage 2 by 50% whilst keeping all other values the same resulted in a change to voltage ratio of -0.2%. In terms of realistic value changes then, we can conclude that a relative life drift in stage 2 values of ±0.5% will give voltage ratio change of ±0.002%, or ±20ppm. Also, a TCR mismatch between stage 2 and the others of ±50ppm/K will contribute just ±0.2ppm/K to the total TCVR.

Sources of variation in voltage ratio are likely to be dominated by in-stage variations in TCR, VCR and drift. Inter-stage variations are not controlled by design but will have a negligible effect.

Layout and Manufacturing

This design strategy assumes standard thick film materials and processes which give typical absolute TCR magnitudes of ±25 to ±100ppm/K, and absolute life drift of ±1%. These may be used to TCVR figures below ±5ppm/K and voltage ratio life drifts within ±0.1%. No special manufacturing materials or processes are required. Whilst the same ink must be used for all elements within a given stage, different inks may be used for each of the stages.

In terms of layout, the design should align the matched resistive elements side by side and at equal spacing, connected at the ends by conductor tracks of matching dimensions and width equal to that of the resistive elements. It may be desirable to orientate the substrate so that the direction of printing and firing processes is orthogonal to the imaginary lines separating similar resistive elements so as to minimise the effect of spatial variations in resistor print thickness or furnace temperature.

To avoid disturbing the balance in properties of individual elements, it may be advantageous to avoid laser trimming of the elements in the initial stage or stages, although a course trim, for example to within ±10%, may be desirable in R_1 in order to gain some degree of control over the input impedance and the power dissipation. But the fine adjustment to obtain the desired voltage ratio may be performed in the output stage where voltage stresses are lowest. A nominally 2:1 output stage with matched resistors may be provided for this purpose, with elements R_5 and R_6. This gives a range of ratio adjustment from the as fired ratio of -50% to +unlimited. A large element size and box cuts should be used for good absolute stability. To balance any instability arising from stresses in film adjacent to the trim, it may be advantageous to trim both elements to some extent.

There are two possible trimming strategies. The first is functional adjustment of output voltage with a calibrated high input voltage. Alternatively, the resistances of the input stages may be measured, a calculation performed, and the output stage resistance ratio may then be trimmed accordingly. With respect to the second method, it is noted that the formation of R_1 in separate elements each with nominal value equal to R_2, and R_3 in separate elements each with nominal value equal to R_4, eases the task of measuring high ohmic values with low uncertainty.

An example layout of a nominally 10 x 10 x 2 = 200:1 divider illustrating the above features, except without coarse trim of R_1, is shown below (Figure 8).

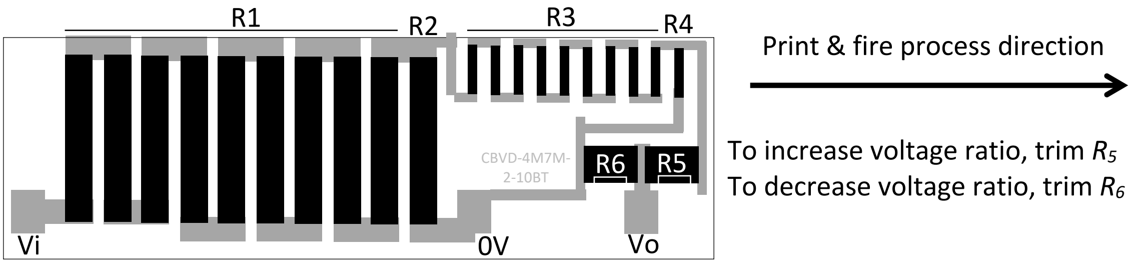

Figure 8 – Three-Stage Cascaded Balanced Divider Layout Example

Note that this layout does not follow the pinout of a conventional two-element voltage divider. For a standard product however, a better approach could be to design the product as pin-compatible with precision conventional products thus supporting second source availability. A suitable layout modification is shown below (Figure 9). This is achieved by using an odd rather than even number of elements in each section. In this example the nominal ratio is reduced to 9 x 11 x 2 = 198:1, but that can still easily be trimmed to 200:1. NB the positions of R_5 and R_6 are transposed.

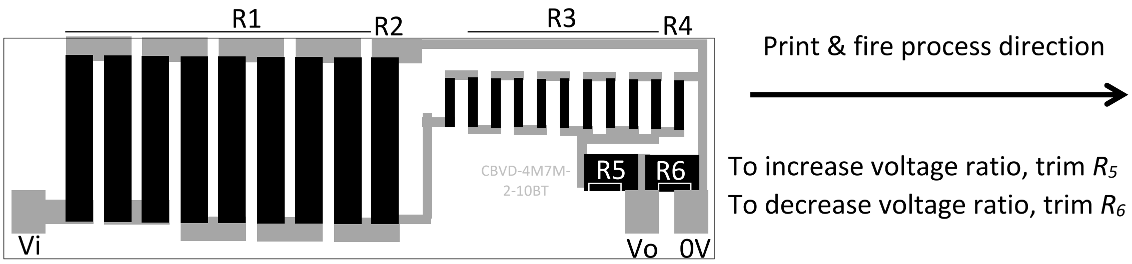

Figure 9 – Alternative Layout Giving Conventional Pinout Order

The loading on the input voltage source is approximately $R_1 + R_2$, and this may be referred to as the input impedance of the CBD. Whilst it would be possible to create a CBD with ±20% tolerance on input impedance and ±0.1% ratio tolerance, in general it will be necessary to bring ohmic value into a ±10% range in order to control power dissipation, and to go at least some way to meet customer expectations of having a reasonable degree of control over loading of the input voltage source. This can be achieved by selective opening of links; the individual elements should not be trimmed by partial removal of film, as this could lead to unbalanced drift in the high voltage stage. An example (Figure 10) shows how one element in a parallel pair may be trimmed open circuit, effectively doubling the resistance of that leg. In a string of 10 elements of value R, two of which are paralleled in this way, the untrimmed value is 8.5R. Such an adjustment takes the value up to 9R, a step of about +6%. With an as-fired range of -30 to +10%, this strategy is therefore suitable to achieve ±10% with the trimming open of up to 4 elements.

Note that the trimming of elements should involve multiple cuts for two reasons: firstly, to restrict voltage stress across cuts to a safe level and secondly, to minimise the parasitic capacitance of the residual material.

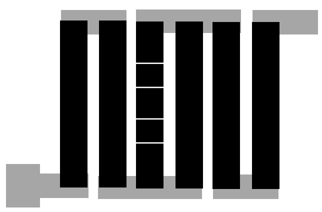

Figure 10 – Example of Coarse Value Trim Strategy

Key Parameters of the Divider

The parameters which need to be set prior to designing a cascaded balanced divider, and typical values are as follows:

1. High voltage rating e.g. typically in the range 1kV to 50kV
2. High voltage division ratio e.g. typically in the range 100:1 to 10,000:1
3. Low TCVR, typically ±15ppm/°C or better
4. Low VCVR, typically ±1ppm/V or better
5. High stability of ratio during life, typically ±0.1% or better
6. High ratio tolerance, typically ±0.1% or better, unless software calibration is used
7. Low effect of parasitic reactances on fast changing voltage levels or ac voltages
8. Simple and rapid bi-directional ratio adjustment method
9. Standard thick film resistor materials and processes

Benefits and Disadvantages of the New Approach

The CBD approach to the design of high voltage dividers promises to enable products which achieve a higher level of precision using conventional manufacturing processes. No special thick film materials are needed, and process controls do not need to be any different from those used for conventional divider manufacture. In particular it does not require direct writing thick film processing nor any form of measure and match process. The trimming process, whilst non-standard, could be automated to run at a rapid rate. The manufacturing costs should therefore be similar to those for conventional divider products.

The disadvantages are the higher complexity of the design task, both in the schematic and print layout stages, combined with the higher output impedance which calls for a high input impedance following stage. For the best stability performance, it is suggested that no fine-trim stage be included and, where this is the case, the product is only suited to applications providing software-based calibration of the voltage measurement. In addition, some market education may be necessary to gain acceptance for a high precision divider with a ratio tolerance of 10%. In practice a finely trimmed output stage may be necessary to trade off stability against market requirements for, or at least expectations of, high ratio tolerance.

REALISATION AND VERIFICATION

Design Targets

The design targets for the test samples were as follows:

1. Voltage rating of 1kV
2. Voltage ratio of 200:1
3. Input impedance of 3M0 ±10%
4. Output impedance ≤250K
5. TCVR of ±10ppm/°C
6. VCVR of ±1ppm/V
7. Life stability of ratio (1000 hours load) of ±0.1%
8. Ratio tolerance trimmable to ±5%
9. Rating 0.5W at operating ambient temperature from -40 to +85°C
10. Substrate size 25.4 x 9.4mm

Design Example

The test sample design which was made for proof-of-concept testing is shown in Figure 11. This design was based on the schematic of Figure 6 and used a standard substrate size of 25.4 x 9.4mm as found in an existing conventional divider product. Terminal P1 is the high voltage input, P2 is ground and P3 is the low voltage output. Provision was made for an additional terminal, P4, which connected to the inter-stage node and permitted separate measurement of the voltage ratios of stage 1 and stage 2. In a finished design this connection is not required, and the space can be filled with the R_1 and R_2 elements, thus optimising for power density and voltage rating.

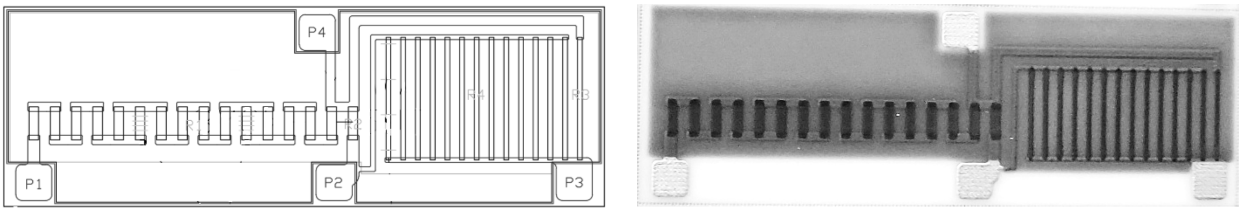

Figure 11 – Test Sample Print Design and Sample Image

The two-stage design was a 14 x 14 = 196:1 divider with the characteristics shown in Table 2:

Res	# Elements	Multiplier [2]	Element Value	Total Value [2]	Abs. Tolerance [2]	Stage Power [1]	Stage Voltage [1]	Stage Voltage Ratio [2]
R1	15	12 (13)	214K	2M57 (2M78)	+10/-20% (±10%)	≥0.36W	≥1000V	14.0 (15.2)
R2	1	1	214K	214K	+10/-20%			
R3	1	1	2M14	2M14	±15%	negligible	≥75V	14.0 (13.0)
R4	13	1/13 (1/12)	2M14	165K (178K)	±15%			

Note 1: the ratings shown are for each entire stage, e.g. R1+R2. The required power rating is 0.5W.
Note 2: the main figure relates to untrimmed case, and the figure in brackets relates to the fully trimmed case.

Table 2 – Resistor Element Parameters for Test Sample

Test Results

The results across a sample of five units are summarised in Table 3. These results are promising in terms of meeting the targets for the two key precision parameters TCVR and VCVR. At the time of writing long-term environmental drift has not been assessed.

Parameter		Target	Result
VCVR	ppm/V	±1	-0.2 typical, -0.35 worst case
TCVR	ppm/K	±10	-1.6 typical, -4.6 worst case
Zin	Ω	3M0 ±10	2M6 typical without trimming
Zout	Ω	≤250K	147K typical
Voltage Ratio		200	203 to 228 without trimming
Absolute VCR	ppm/V	None set	-0.82 worst case
Absolute TCR	ppm/K	None set	+34.6 worst case

Table 3 – Test Results Summary

To assess the performance in the light of the actual element linearity, and to eliminate the possibility that this happened to be better than normal for the samples manufactured, the absolute VCR and TCR of the high voltage stage (R_1 and R_2) were also measured. Comparison between the VCVR and absolute VCR gives an indication of the value of a balanced design strategy, with the ratio error being typically only 25% as great as the absolute error. For TCVR the ratio error was below 5% of the absolute error.

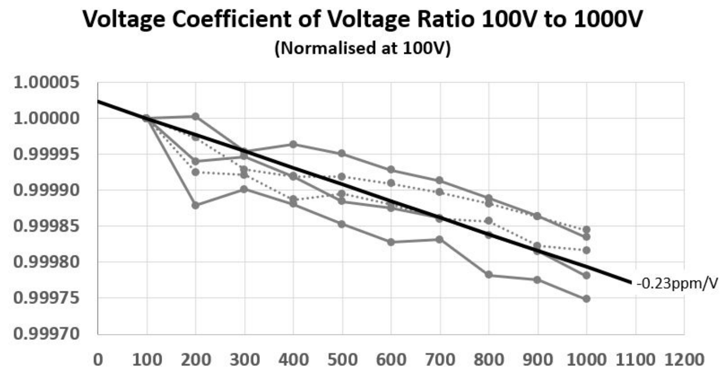

Figure 12 – Voltage Linearity Results

Looking in more detail at the voltage linearity, in Figure 12, the ratio error is plotted against applied voltage, normalised to the ratio at a reference measurement voltage of 100V. The mean value is -0.23ppm/V and from 400V to 1000V all the characteristics track this gradient closely. The behaviour in the range below 400V shows greater spread. Further work needs to be done to establish the reason for this.

Future Work

The next generation of samples should serve to support investigation of four areas in which improvement or fuller characterisation of performance are required.

1. AC performance – all testing so far has been at DC, which supports applications such as battery monitoring and defibrillator charge control. Characterisation at least at power line frequencies would extend the application areas. It would be interesting to establish whether any benefit may be detected from the matching of parasitic reactances in the balanced design of each stage. As conventional divider datasheets do not normally publish data on this aspect of performance, such testing should include conventional design dividers as a benchmark.

2. Trimming – the first samples were untrimmed since they were for basic proof of concept. Both coarse and fine trimming should be included in the next designs with testing of performance with and without trimming applied. This will indicate the extent of the potential stability cost of including fine trim, as well as confirming the control possible over input impedance and ratio tolerance.

3. Layout – as terminal P4 may be dispensed with, future designs can optimise the track layout so that the resistive elements are as large as possible. This will reduce power density and voltage stress in the film and allow the use of lower resistivity inks which should in turn improve all aspects of precision performance.

4. Drift and Ratings – The load life drift needs to be established, and this should be done at multiple rating levels in order to establish the power density level at which the performance can match or exceed the best-in-class products.

CONCLUSIONS

The cascaded balanced divider approach for creating thick film high voltage dividers appears to promise a step change in precision and stability with little or no effect on manufacturing cost relative to conventional dividers. The first samples designed by this method are being evaluated and the results of testing sensitivity to temperature and voltage are encouraging. The voltage sensitivity equals that of the best available conventional dividers whilst temperature sensitivity is improved over conventional dividers by a factor of two. Opportunities to optimise this design in a way that will improve the voltage sensitivity have been proposed and next steps towards a practical product design have been identified.

REFERENCES

[1] Direct-Write Precision Resistors for Ceramic Packages; P Yang et al; Ceramic Technologies Research; Dec 1988

[2] https://www.semanticscholar.org/topic/Kelvin%E2%80%93Varley-divider/2424503

[3] A Voltage Divider Standard; L. C. Fryer; Published in Transactions of the American Institute of Electrical Engineers – Part 1 Communication and Electronics; May 1962