6.2. Experimental Evaluation of Wear Failures in SMD Inductors

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ABSTRACT

In recent years, the advancement of electronic devices in mobility has made ensuring signal integrity and addressing EMI increasingly important. Our inductors are being adopted more frequently by Tier 1 suppliers. During the component certification process, we receive requirements equivalent to lifespan evaluations known as Mission Profile assessments. To conduct a Mission Profile assessment, it is necessary to evaluate the worst-case risk failure mode and its activation energies. We have been conducting research on wear failure modes in SMD inductors, and we will present our findings on this topic.

Introduction

Mission Profile Validation on Component Level

The electrification of the automotive industry has rapidly progressed in recent years, driven by societal demands for sustainable mobility and advances in autonomous driving technologies. As vehicles are expected to operate for longer durations and under a wider variety of conditions, ensuring the long-term reliability and robustness of automotive electronic components has become increasingly critical. In response, manufacturers are adopting robust design philosophies and extending warranty periods, with component lifetimes of 10 or 15 years, and even 20 years, becoming commonplace.

To address these challenges, the concept of a “Mission Profile” has been introduced. A Mission Profile represents a simplified description of the environmental and operational conditions that automotive components are expected to encounter throughout their service life. Standardization bodies, such as those responsible for the AEC-Q100 qualification for integrated circuits, have incorporated Mission Profile assessments into their reliability evaluation procedures.

Despite the growing importance of Mission Profile-based validation, there remains a lack of detailed studies examining failure mechanisms at the component level, particularly for surface-mounted device (SMD) inductors such as multilayer ferrite beads. In this paper, we report on the experimental evaluation of wear failure mechanisms of multilayer ferrite beads, under high-temperature current load testing.

references [1], [2], [3]

Experimental Setup

The schematic diagram of the multilayer ferrite bead used as the Inductor Under Test (IUT) is shown in Fig. 1(a). The IUT was prototyped specifically for this experiment. The ferrite core was fabricated by stacking ferrite sheets, while the inner coil electrodes were formed by screen-printing Ag paste. To verify the effect of current acceleration, a simple structure with two straight internal coil layers was employed. The external electrodes were formed by dipping in Ag paste, followed by firing, and subsequent electroplating with Ni and Sn layers in sequence. In this paper, these are referred to as the Ag paste layer, Ni plating layer, and Sn plating layer, respectively. The IUT dimensions are 1.6 mm × 0.8 mm × 0.6 mm.

The fabricated IUTs were soldered onto □14 mm evaluation boards. The solder paste used was Sn-3.0Cu-0.5Ag, and it was applied at a thickness of 150 μm. Multiple boards were connected in a daisy chain using φ1.4 mm copper wire.

The evaluation boards were placed in a thermostatic chamber at 150°C (423 K). 10 A was applied using a DC power supply. Given that the rated current of ferrite beads of this size is generally below 1 A at 150°C, the applied condition represents a highly accelerated and severe stress. The IUTs were periodically removed, and their DC resistance was measured at room temperature. In addition, cross-sectional polishing was performed on selected samples, and cross-sectional observation was conducted using a digital microscope and SEM-EDX.

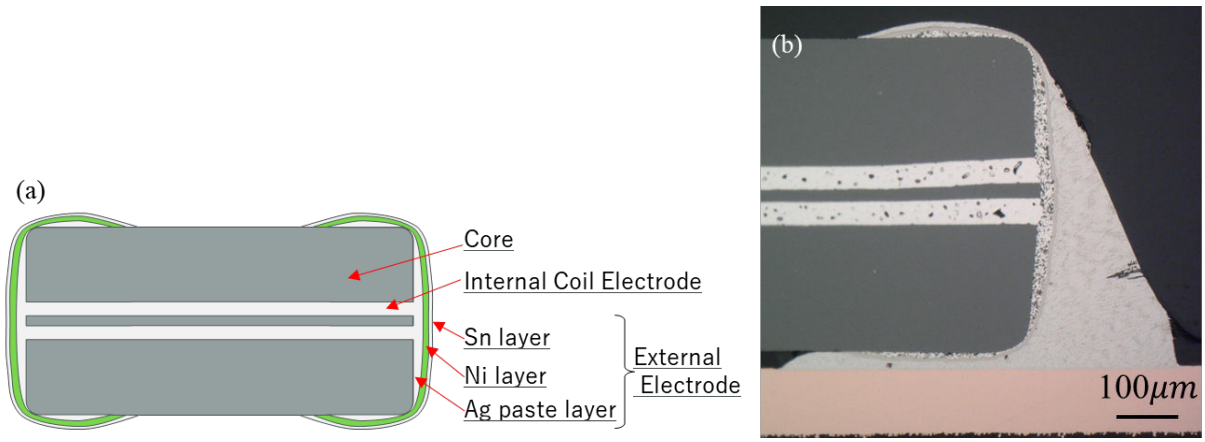

Fig.1. Cross-sectional images of the ferrite bead; (a) schematic diagram, (b) initial state of IUT.

Results and Discussion

Initial state

Fig. 1(b) shows part of the cross-sectional image of the IUT in its initial state. In this paper, images are presented with the direction of electron flow from left to right, with the left side (electron inflow) referred to as the anode, and the right side (electron outflow) as the cathode.

Variation in DC resistance

Fig. 2 shows the change in DC resistance. There was no significant change up to approximately 200 hours. After 200 hours, the DC resistance exhibited an increasing trend.

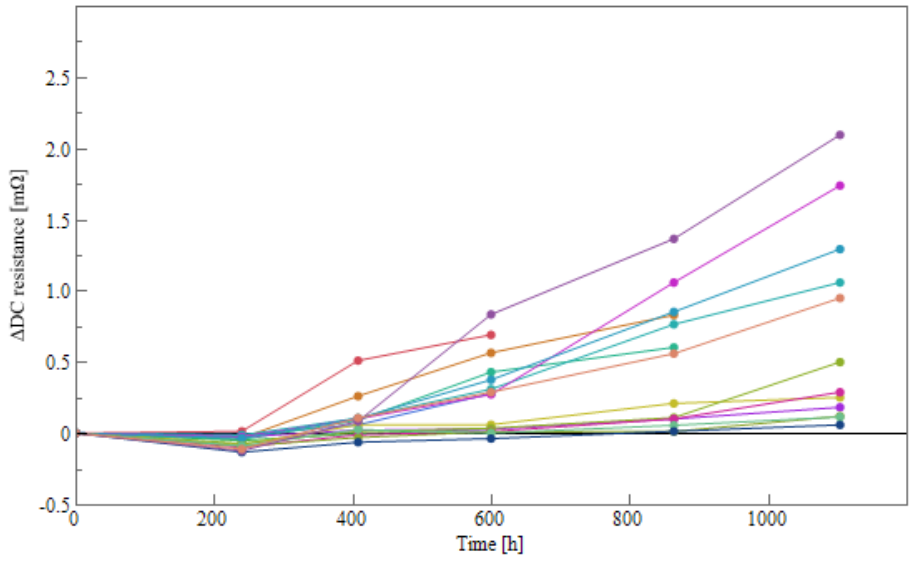

Fig.2. Variation in DC resistance; measurements were taken after removal at room temperature.

Cross-sectional SEM-EDX image

Cross-sectional SEM images are shown in Fig. 3. On the cathode side, the Ni plating layer, which was initially of uniform thickness, was partially thinned and depleted in some areas. Voids were also observed along the external electrode. In contrast, the Ni plating layer on the anode side remained uniform, and the IMC (intermetallic compound) layer was thicker compared to the cathode.

SEM-EDX images are shown in Fig. 3. On the anode side, IMC layers of Cu and Sn were deposited along the Ni plating layer of the IUT, extending from the substrate land to the height of the coil electrode. On the cathode side, IMC layers of Cu and Ni with Sn were deposited outside the solder fillet. In the vicinity of the coil electrode, the Ni plating was partially depleted. In regions adjacent to the depleted Ni plating, Sn had diffused into the Ag paste layer, forming IMC. Voids were observed at the interface between the Ni–Sn IMC and the solder.

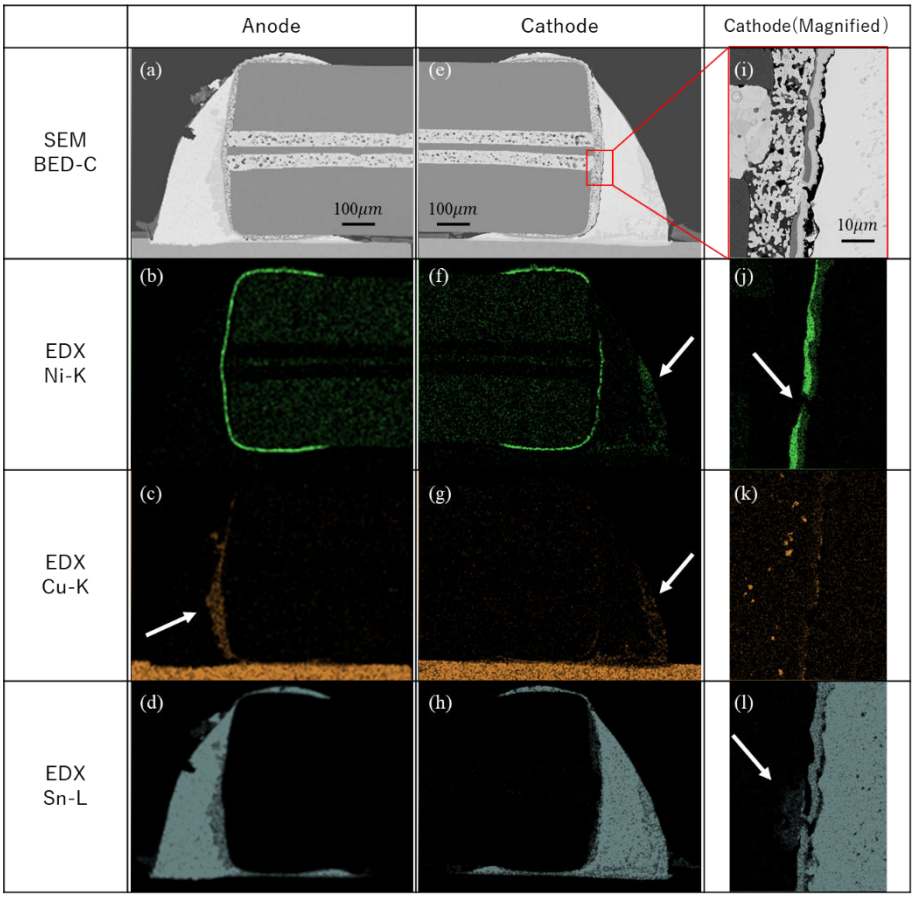

Fig.3. Cross-sectional SEM-EDX image of sample after 600 hours. (a)-(d)Anode, (e)-(h)Cathode, (i)-(l)Magnified view of Cathode.

Discussion

Since the locations where Cu and Ni are deposited depend on the polarity of the electric current, these phenomena are considered to be promoted by electromigration. The void formation observed at the cathode is also a known effect of electromigration. On the anode side, electrons flow from the substrate land toward the chip inductor, causing Cu from the land to diffuse toward the chip. On the cathode side, electrons flow from the chip inductor to the substrate land, resulting in Cu diffusing into the solder fillet, and Ni from the external electrode's Ni plating diffusing toward the substrate land. Consequently, parts of the Ni plating layer were found to have disappeared. On the anode, the absence of changes in the Ni plating layer may be due to the fact that electromigration-driven Ni diffusion is directed toward the Ag paste layer of the external electrode, with which Ni doesn't form alloys. It has been reported that the diffusion coefficient of Ni varies significantly depending on the crystallographic orientation of Sn, and therefore the sites of deposition are expected to be scattered.

The observed increase in Rdc over time is attributed to the formation of intermetallic compounds resulting from Sn diffusion into the Ag paste layer adjacent to regions where the Ni plating had disappeared. Since intermetallic compounds typically have higher resistivity than pure metals, the further the IMC region extends into the Ag paste layer or coil electrodes due to Sn diffusion, the greater the increase in DC resistance of the IUT. Additionally, the occurrence of voids along the cathode external electrode is considered another factor contributing to the rise in DC resistance. A further increase in resistance can lead to thermal runaway due to chain-reaction heating, ultimately resulting in open failure.

references [4], [5], [6]

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SUMMARY AND CONCLUSIONS

In this study, we investigated the wear failure mechanisms of SMD inductors, specifically multilayer ferrite beads, under high-temperature current load testing. Under highly accelerated conditions of elevated temperature and large current, polarity-dependent diffusion phenomena due to electromigration were observed. On both the anode and cathode sides, Cu and Ni were found to be deposited in the solder at locations corresponding to the direction of electron flow. Partial depletion of the Ni plating layer on the external electrode was also observed. From these regions, Sn was found to diffuse into the Ag paste layer of the external electrode. The primary cause of the increase in DC resistance is considered to be the formation of these intermetallic compounds. Additionally, voids were observed at the interface between the Ni–Sn intermetallic compounds formed adjacent to the Ni plating layer and the solder. This void formation is also regarded as a contributing factor to the rise in DC resistance. As diffusion progresses further, the DC resistance is expected to increase more significantly, ultimately leading to thermal runaway and open failure. Ongoing work will focus on investigating the detailed mechanisms, establishment of acceleration models, and development of countermeasure technologies.

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